Signal and Power Integrity Analysis of DDR4 Address Bus of Onboard Memory Module

Anil Pandey
Keysight Technologies, RnD
Presentation Outline

- DDR4 Signal Groups
- High Speed Design Challenges
- Address Bus SI-PI Analysis Flow
- Address Bus Power Integrity Analysis
- Address Bus Layout Design and Routing
- DC/AC Simulation and Result
- Electro-Thermal Analysis
- Power Aware SI Simulation of Address Bus
DDR4 Memory: Xilinx FPGA Board

**FPGA:** Kintex XCKU040-2FFVA1156E FPGA
- ROHS compliant KCU105 kit including the XCKU040-2FFVA1156E FPGA

**Memory:** Micron EDY4016AABG-DR-F-D
- 2GB DDR4 component memory (four [256 Mb x 16] devices) at 1200MHz / 2400Mbpsps

The 2 GB DDR4 component memory system is comprised of four 256 Mb x 16 DDR4 SDRAM devices (Micron EDY4016AABG-DR-F-D) located at U60-U63. This memory system is connected to the XCKU040 HP banks 44, 45, and 46. The DDR4 0.6V VTT termination voltage (net DDR4_VTT) is sourced from the TI TPS51200DR linear regulator U24. The connections between the DDR4 component memories and the XCKU040 banks 44, 45, and 46 are listed.
The SI/PI analysis presented here, focuses on the design of the physical layer interface that facilitates communication between the DDR4 module and its controller.
High Speed Design Challenges

1. Signal Quality of Net:
   - Signal distorts due to frequency dependent losses.
   - Receiver circuits fails to distinguish between 1 or 0 logic.

2. Crosstalk:
   - Caused due to mutual capacitance or inductance between two or more signals.
   - Occurs mostly when signals travel parallel to each other for long distances.

3. Jitter:
   - Deviation from ideal clocking position (Power Supply Injected Jitter)
Design Flow

- High Speed Digital Board Layout Design
- Power Integrity
  - DC Simulation of Power Nets (IR Loss)
  - AC Simulation of Power Nets (PDN Impedance profile)
- Connector
  - USB Type-C Connector CAD Model
- Signal Integrity Analysis
  - Transient Analysis: IBIS-AMI Model of TX and RX + 3D Connector Model + USB Data Bus

Optimize Design

Yes

No
Address Bus Power Integrity Analysis

Static IR Drop
- Voltage Drop
- Current Densities

AC Analysis (Dynamic IR Drop)
- Decoupling / Target Impedance
- Plane Noise

Resistor for the metal loss of current distribution path

Plate Capacitor is formed by the Power Plane and GND Plane
Address Bus Layout Design and Routing

An internal channel from the CPU to memory across which the addresses of data (not the data) are transmitted. The number of lines (wires) in the address bus determines the amount of memory that can be directly addressed as each line carries one bit of the address.
DC Simulation Result – Voltage Drop (Compliance)

**[Analysis 1]: Voltage (V)**

1.16 1.17 1.17 1.18 1.18 1.18 1.19 1.19 1.2

- **V\_REF 1.2V**
- **V\_DROP 1.164V (3% tolerance)**
- **V\_DROP 1.14V (5% tolerance)**
- **V\_Drop\_actual 1.16V**

- **With 5% Margin Voltage drop is passing**
- **With 3% Margin Voltage drop is failing**

### Table: Simulation Results

<table>
<thead>
<tr>
<th>Sinks</th>
<th>Pins</th>
<th>VRM</th>
<th>VDD</th>
<th>Reports</th>
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</thead>
<tbody>
<tr>
<td>sink_U1</td>
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<td>1.2</td>
<td>1.16062</td>
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<td>1.2</td>
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<td>0.05</td>
</tr>
</tbody>
</table>

- **Sink : U1**
  - **1.164V**
  - **V\_drop= 36 mV**

- **Controller IC**
  - **VRM: U9**
  - **1.2V**

- **Memory Blocks**

**Power Net 1.2V**
AC Simulation of Power Plane

- AC PI concerns the delivery of AC current to mounted devices to support their switching activity while meeting constraints for transient noise voltage levels within the power delivery network (PDN).
- AC PI is governed by voltage regulator modules, loop inductances, decoupling capacitors (decaps), and plane capacitance.

\[
Z_{\text{Target}} = \frac{\Delta V_{\text{Voltage Tolerance}}}{\Delta I} = \frac{V_{\text{CC}} \times \text{Ripple}\%}{\text{Current Transient}}
\]

\[
\text{Target Impedance} = \% \text{Ripple} \times \frac{V_{\text{CC}}}{(\text{Sink Current})_{\text{Max}}}
\]
AC Simulation Result – PDN Plot without Decaps

“Target impedance” profiles are applied as PI constraints. Lower impedance corresponds to lower transient noise.
AC Simulation Result – PDN Plot with Decaps

- It is difficult to get a reliable reference to capacitor quantity only by experience.
- AC simulation get an effective power solution by iterating capacitor quantity and distribution.

![Graph showing AC simulation results with PDN plot and decaps showing impedance (Z) target at different frequencies.]
Electro-Thermal Analysis

- The electro-thermal analysis performs a thermal aware IR Drop analysis.
- It computes the voltage, IR drop, current, power loss density, and temperature distribution in a PCB taking into account the Joule losses in the metallization and the heat generation by the components.
- The heat is transferred away from the sources to the surrounding ambient by conduction through materials, convection with surrounding air, and direct radiation.
- It leads to a temperature rise in the components and the PCB, what in turns leads to an increase in electrical resistance of the metallization.
Thermal and Electro-Thermal Analysis

Thermal Only Analysis

Temperature rise : 5 deg C

Electro-Thermal Only IR Drop Analysis
Thermal and Electro-Thermal Analysis Result

No Thermal Aware

![Diagram](image)

VCC1V2_FPGA_U1
\[ V_{\text{nom}} = 1.20 \text{ V} \]
\[ I = 1.60 \text{ A} \]

VCC1V2_FPGA_U60
\[ V_{\text{nom}} = 1.176 \text{ V} \]
\[ I = 23.6 \text{ mA} \]

\[ V_{\text{pp}} = 22.9 \text{ mV} \]
\[ V_{\text{pg}} = 0.7 \text{ mV} \]

VCC1V2_FPGA_U61
\[ V_{\text{nom}} = 1.176 \text{ V} \]
\[ I = 23.6 \text{ mA} \]

\[ V_{\text{pp}} = 23.6 \text{ mV} \]
\[ V_{\text{pg}} = 0.7 \text{ mV} \]

\[ \Delta V = +0.2 \text{ mV} \]

+0.2 mV

+0.2 mV

+0.3 mV

Thermal Analysis

VCC1V2_FPGA_U1
\[ V_{\text{nom}} = 1.20 \text{ V} \]
\[ I = 1.60 \text{ A} \]

\[ V_{\text{pp}} = 24.0 \text{ mV} \]
\[ V_{\text{pg}} = 0.8 \text{ mV} \]

VCC1V2_FPGA_U60
\[ V_{\text{nom}} = 1.176 \text{ V} \]
\[ I = 23.6 \text{ mA} \]

\[ V_{\text{pp}} = 23.2 \text{ mV} \]
\[ V_{\text{pg}} = 0.8 \text{ mV} \]

VCC1V2_FPGA_U61
\[ V_{\text{nom}} = 1.176 \text{ V} \]
\[ I = 23.6 \text{ mA} \]

\[ V_{\text{pp}} = 23.2 \text{ mV} \]
\[ V_{\text{pg}} = 0.8 \text{ mV} \]

\[ \Delta V = +0.2 \text{ mV} \]

+0.2 mV

+0.3 mV

+0.3 mV
Power Aware IBIS v5.0 Models

- IBIS (Input/output Buffer Information Specification) models are behavioral using I-V and V-t look-up tables that make simulations extremely fast.
- There are two BIRDs related to the power awareness of the IBIS v5.0 models:
  - The first power aware BIRD is 95.6: Power Integrity Analysis using IBIS.
  - The second power aware BIRD is 98.3: Gate Modulation Effect.

**RX IBIS Model**

**TX IBIS Model**
Address Bus S-Parameter Simulation Result
VTT Power Plane: PI-AC Simulation (With Decaps)
Power Aware SI Simulation of Address Bus
Address Bus Power Aware SI Simulation: Result

DDR4_A0

A0_U1

A0_U63

A0_U62

A0_U61

A0_U60

R 238

VTT

Address Bus Power Aware SI Simulation: Result
Address Bus Power Aware SI Simulation Result
(with and without Power Aware)

Blue - Without Power Plane
Red - With Power Plane (Power Aware SI)
Address Bus Eye Diagram  (Power Aware SI Simulation )

Control and Commands

All Other Address Bus Control Signals
Conclusion

- A transient co-simulation methodology is presented on FPGA board design to characterized DDR4 address bus based on power and thermal-aware signal integrity analysis.
- This analysis approach can be extended in high-speed SerDes designs (like PCIe, USB, HDMI) also.